VERSION WITH MARKINGS TO SHOW CHANGES MADE

[0006] (Amended) Unfortunately, due to the complexity of modern IC layouts, detecting and correcting this type of layout imperfection (a technique sometimes referred to as "layout beautification") can be difficult. A method sometimes used to eliminate notch-type imperfections involves applying an oversizing/undersizing technique to entire polygons using a DRC tool. As indicated in Fig. 1d, each edge of polygon 100 is biased outward (oversized). As this biasing takes place, notch 111 formed by edges 102-104 shrinks and eventually disappears. The remaining edges can then be biased inward (undersized) to create a corrected (un-notched) polygon having the same overall dimensions as the original polygon 100.[, as an intermediate polygon 150 is formed, as shown in Fig. 1e (the dashed outline of original polygon 100 is depicted for reference). Polygon 150 includes edges 106-109 forming a rectangle, with edge 109 replacing edges 101-105 in polygon 100. Each of edges 106-109 is then biased inward (undersized) by the same amount as the original outward bias to form a corrected polygon 160, shown in Fig. 1f.]

[0015] (Amended) Figs. 1a-1d[f] show an example layout imperfection (notch) and a conventional method of correcting such a layout imperfection;